Foldback Current Limiting Design and Optimization for Hot-Swap and E-Fuse ICs

Wenjing Zhang, ON Semiconductor

Basic Info of Wenjing Zhang

Sr. Principal Application Engineer
ON Semiconductor

PhD in Microelectronics & Solid State Electronics, 2007-2010
Master in Physics, 2004-2007
Bachelor in Mechatronics, 1997-2001

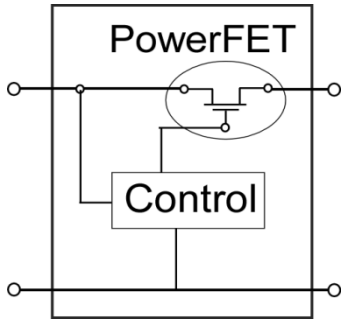
Main Responsibilities

- To carry out the new product definition.
- To provide 2nd level (local expert) technical support.
- To support marketing activities.
- To involve in local design-in activities.
- To make technical documents and training.
- To validate product and generate report.

HotSwap & eFuse

What?

Integrated Overcurrent, Overvoltage, Reverse-Current and Short Protection



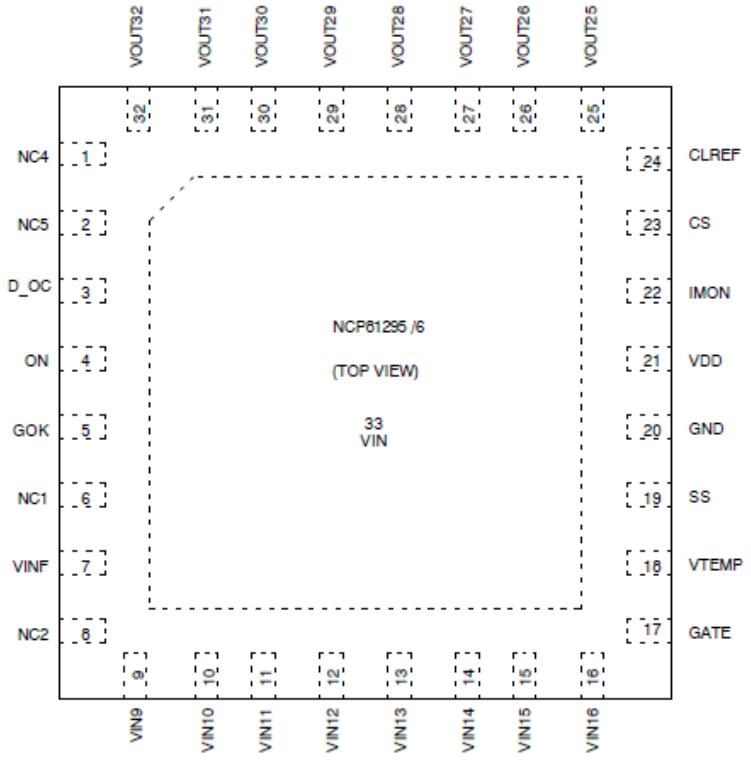
Why?

Prevent damage **to connectors, PCB traces and downstream components**

Where?

Any *hot-plug application* and any system requiring *inrush/outrush current limiting*

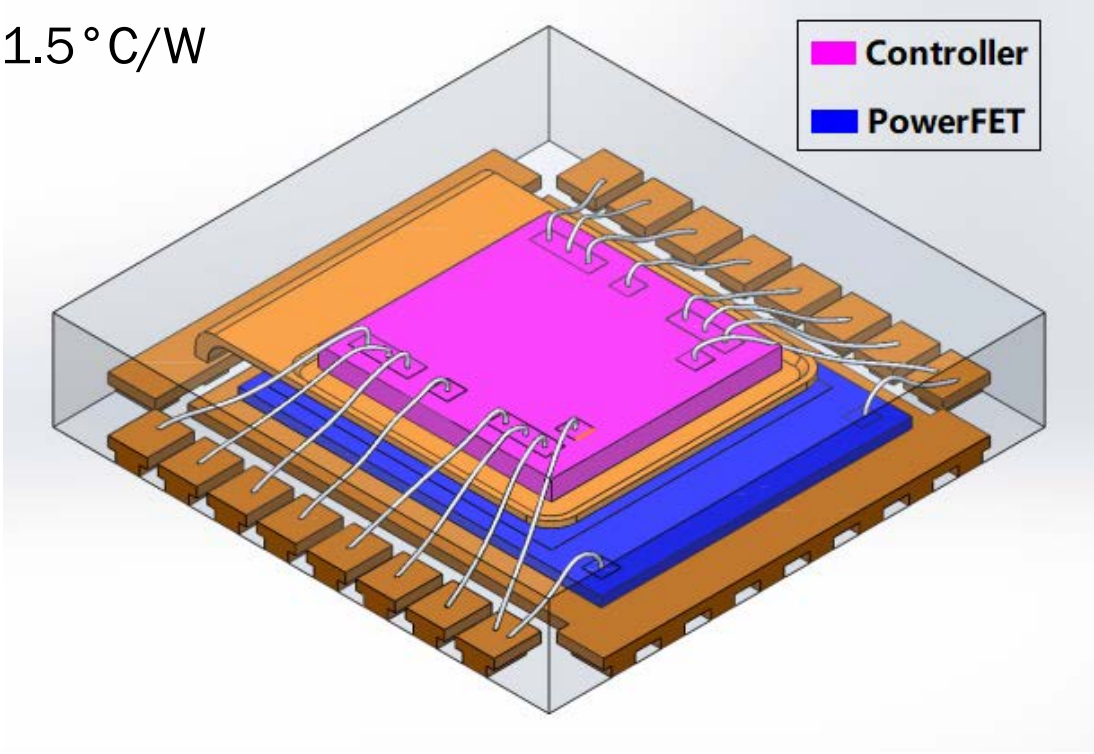
NCP81295/6 – 12V/50A Hotswap IC from ON Semi



Standard 5mm X 5mm LQFN Package

0.65mΩ SenseFET

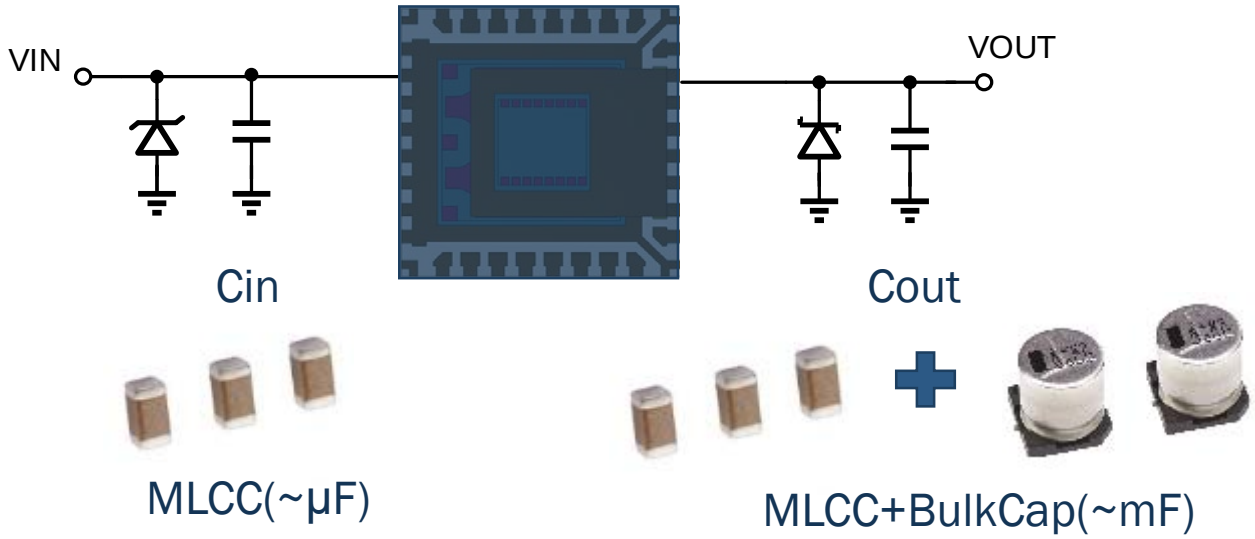
$R_{\theta JB}$ = 1.5 °C/W



Soft-start in Applications

Applications

- servers
- storage
- base band unit
- 12V backplanes



T_{SS} is fixed for certain application condition:

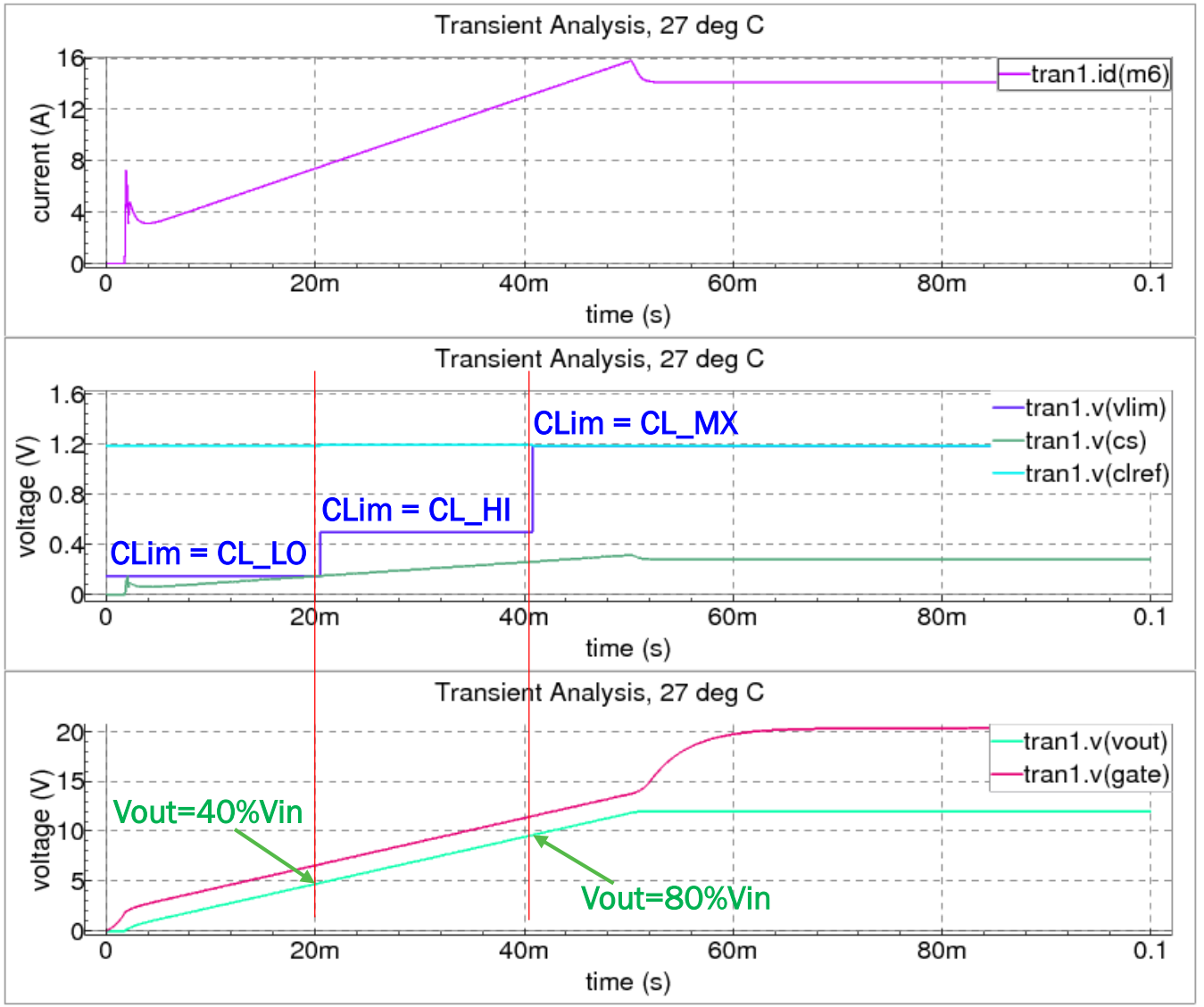
$$\frac{dV_{OUT}}{dT} = constant$$

3-stage current limit with different VOUT for SOA operation in soft start.

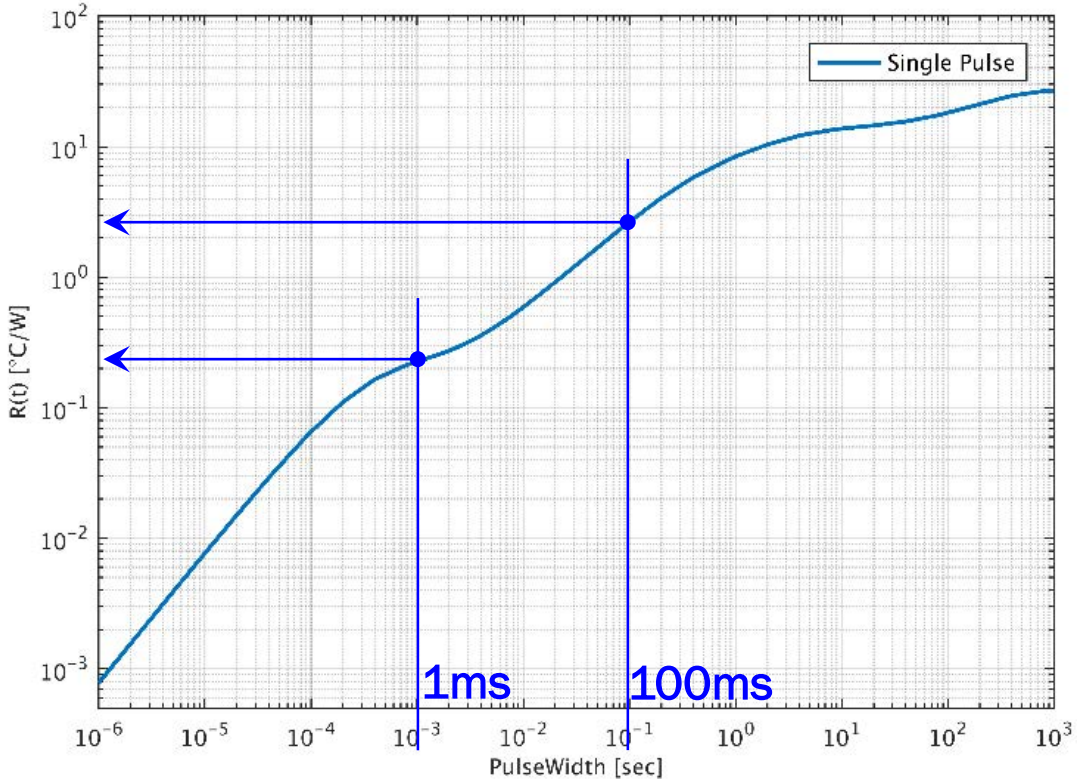
3-stage Current Limit

3-step current limit strategy:
the 3 low levels for SOA operation;
the highest level for fully ON DC operation (programmed by external resistor).

CLim	VOUT
CL_LO	VOUT < 40%VIN
CL_HI	40%VIN < VOUT < 80%VIN
CL_MX	VOUT > 80%VIN,

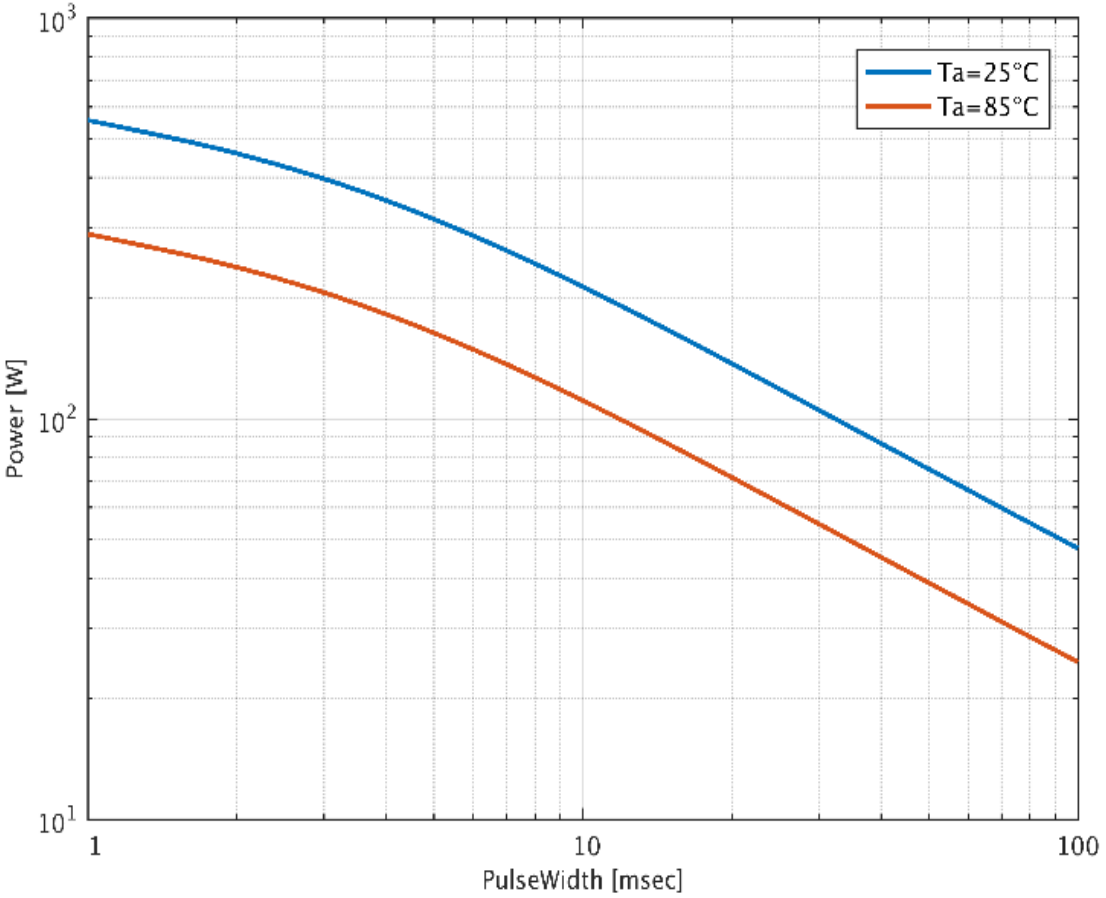


How to define CL_LO/HI/MX



The maximum single pulse power dissipation:

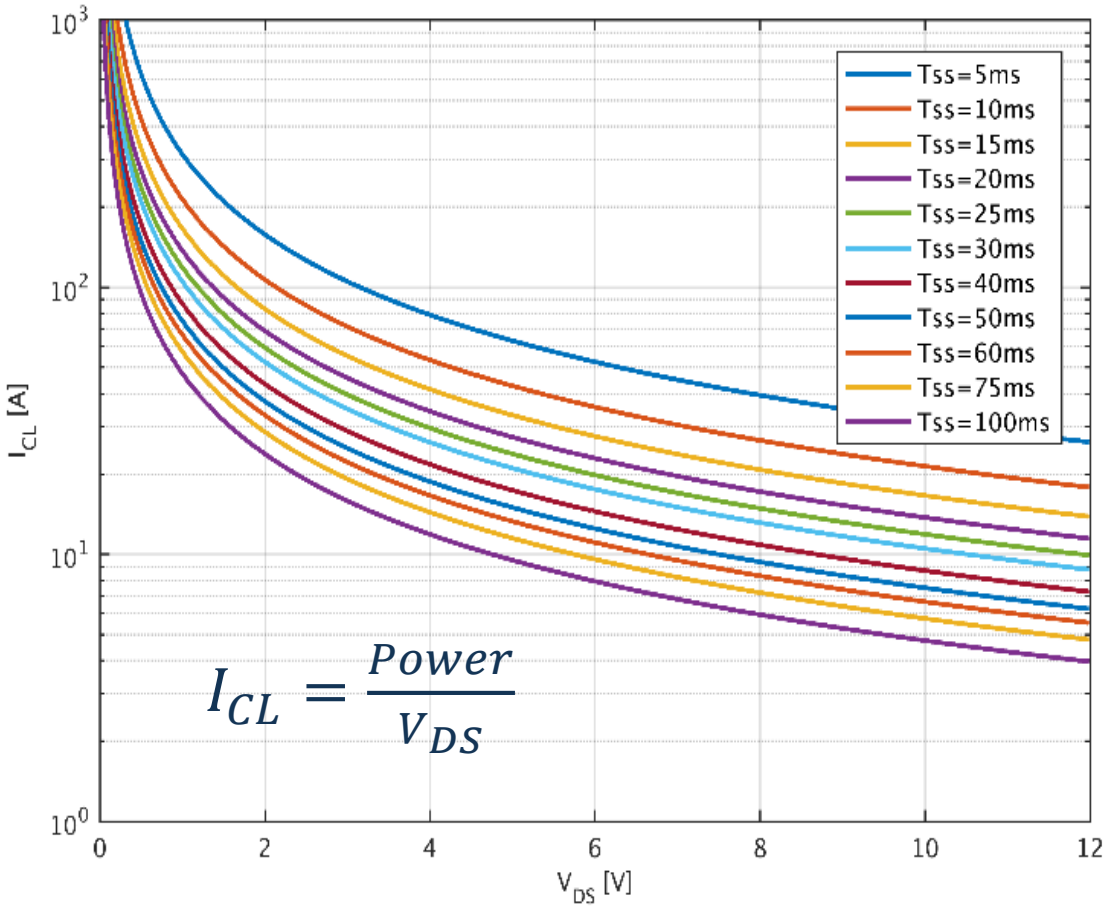
$$Power = \frac{T_{jmax} - T_a}{R(t)}$$

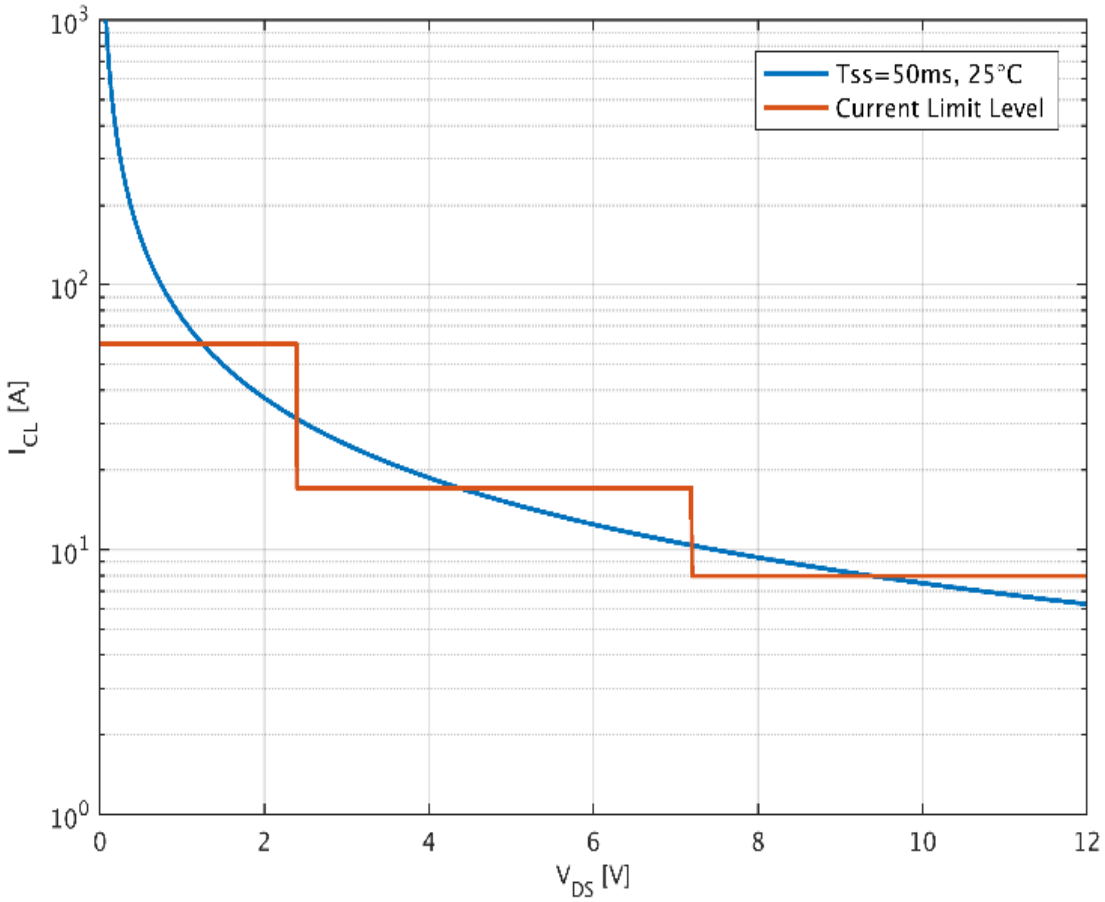


The maximum single pulse power dissipation curves (T_{SS} = 1ms –100ms）

where R(t) is the junction-to-ambient transient thermal impedance and Tjmax is the maximum allowed junction temperature of the MOSFET

How to define CL_LO/HI/MX

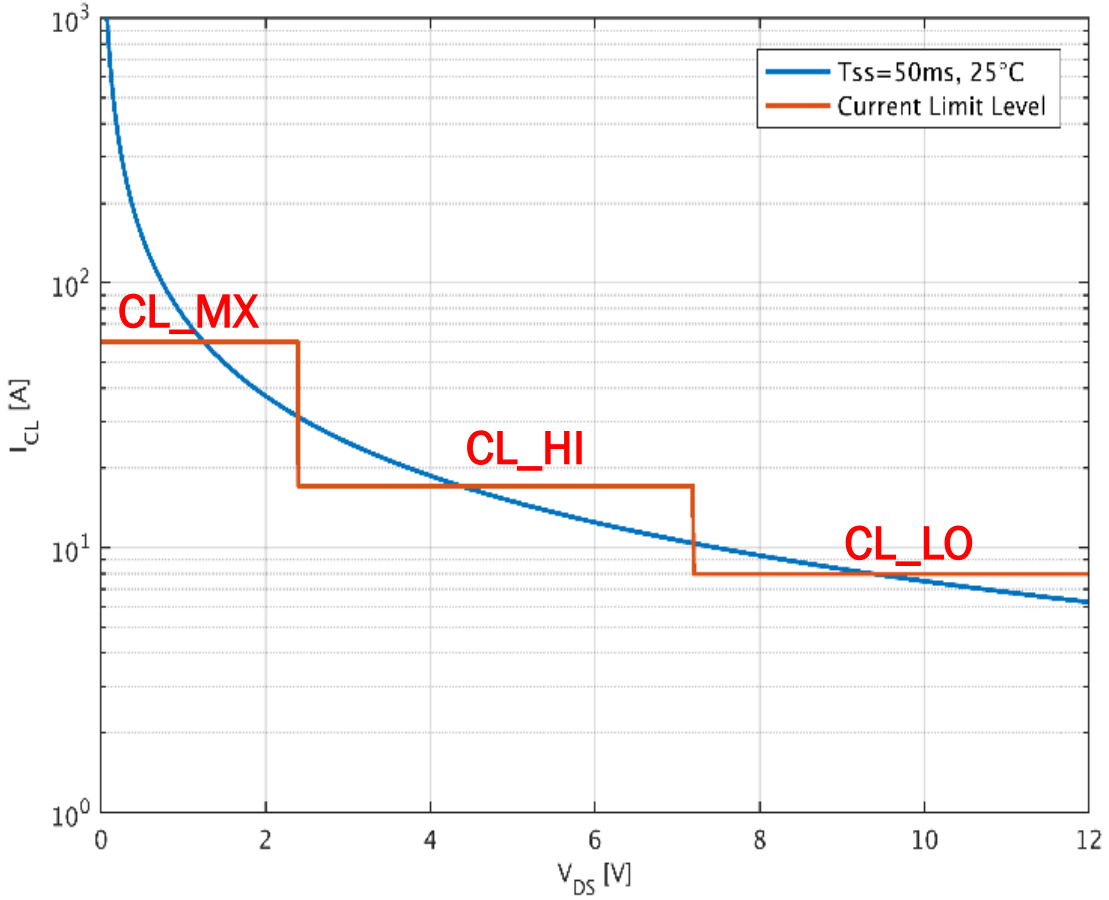




The current limit curves for different soft-start time (Ta = 25°C)

$$I_{CL} = \begin{cases} \langle I_{CL} \rangle, & V_{DS} < 40\% V_{IN} \\ \langle I_{CL} \rangle, & V_{DS} = 40 - 80\% V_{IN} \\ 50A, & V_{DS} > 80\% V_{IN} \end{cases}$$

How to define CL_LO/HI/MX



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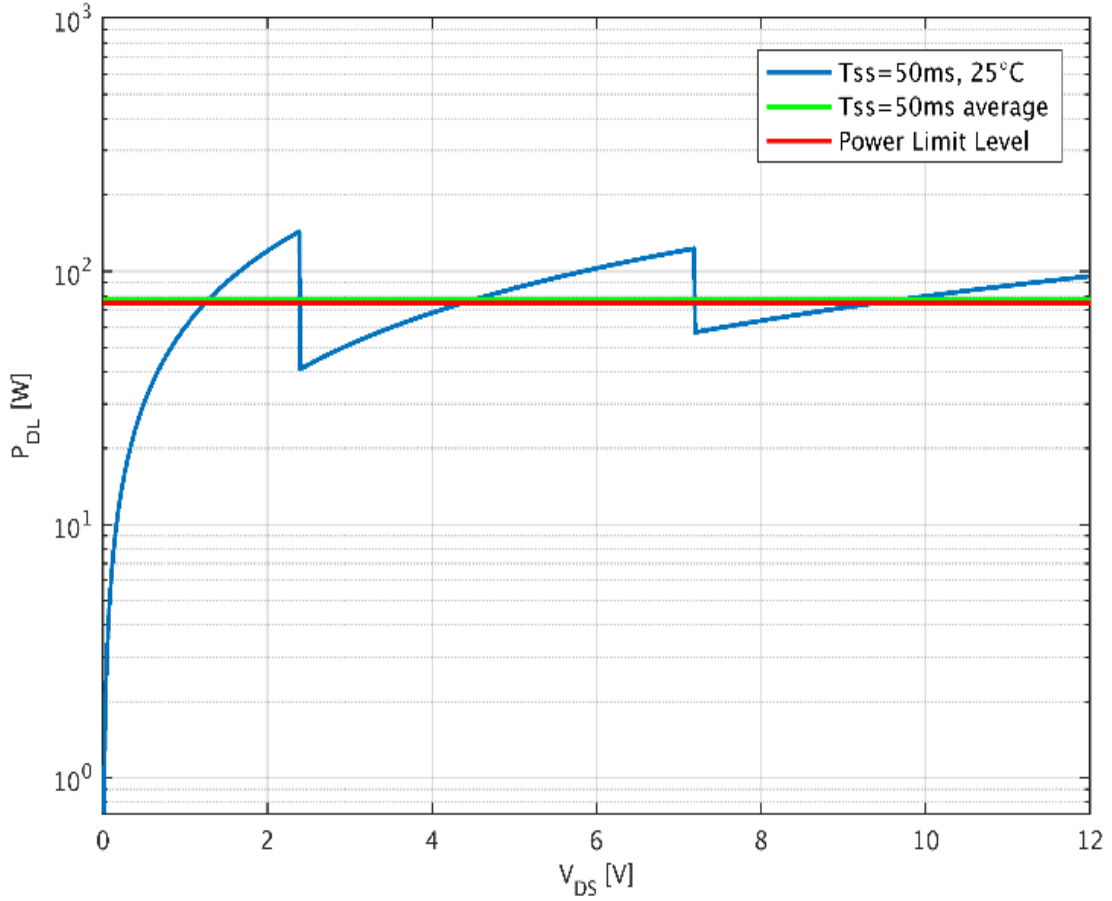


$$P_{DL} = I_{CL} \times V_{DS}$$

Optimization for Electro-Thermal Instability

the drain current on temperature increase:

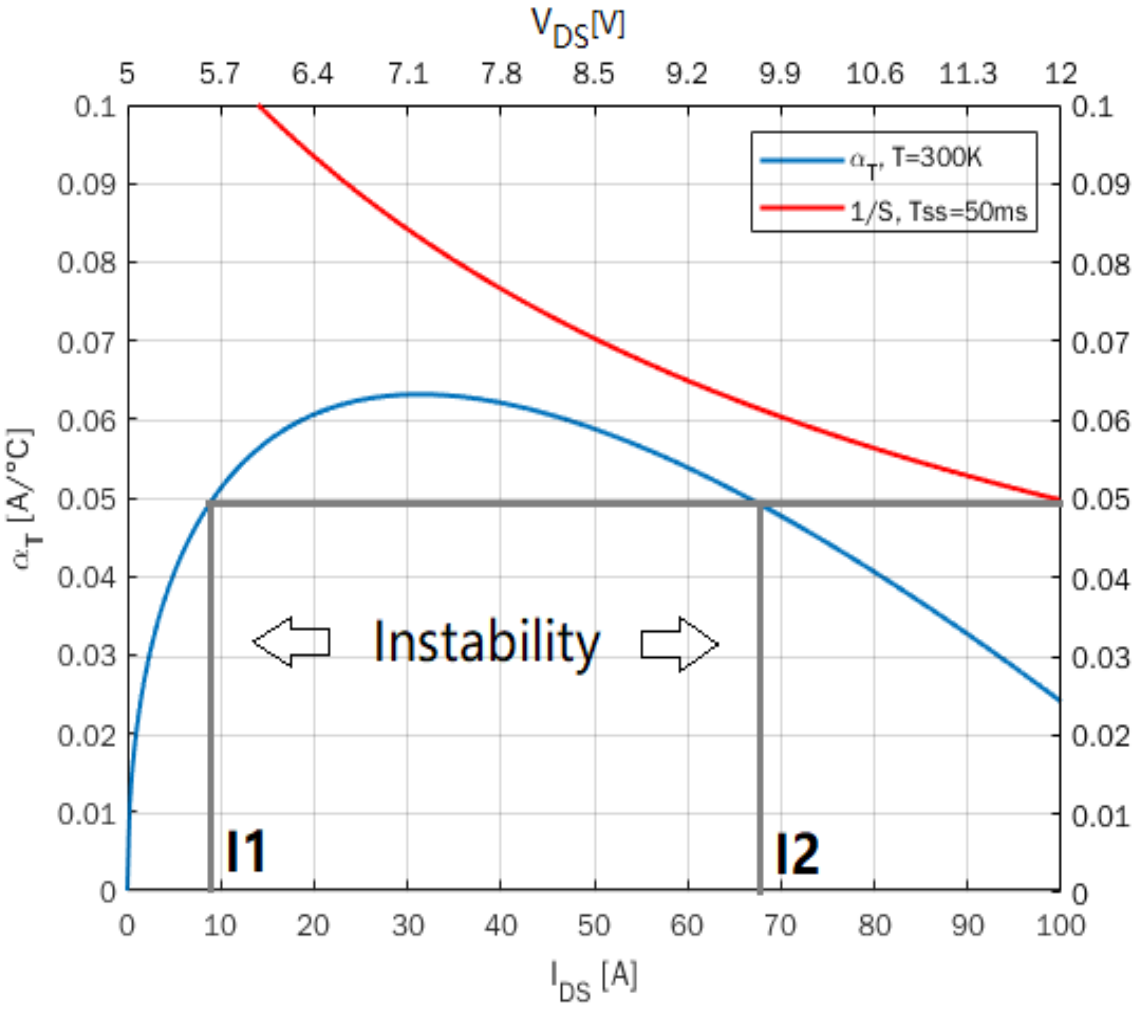
$$I_D(T_{jmax}) = I_D(T_a) + \alpha_T(T_{jmax} - T_a)$$

the junction temperature:

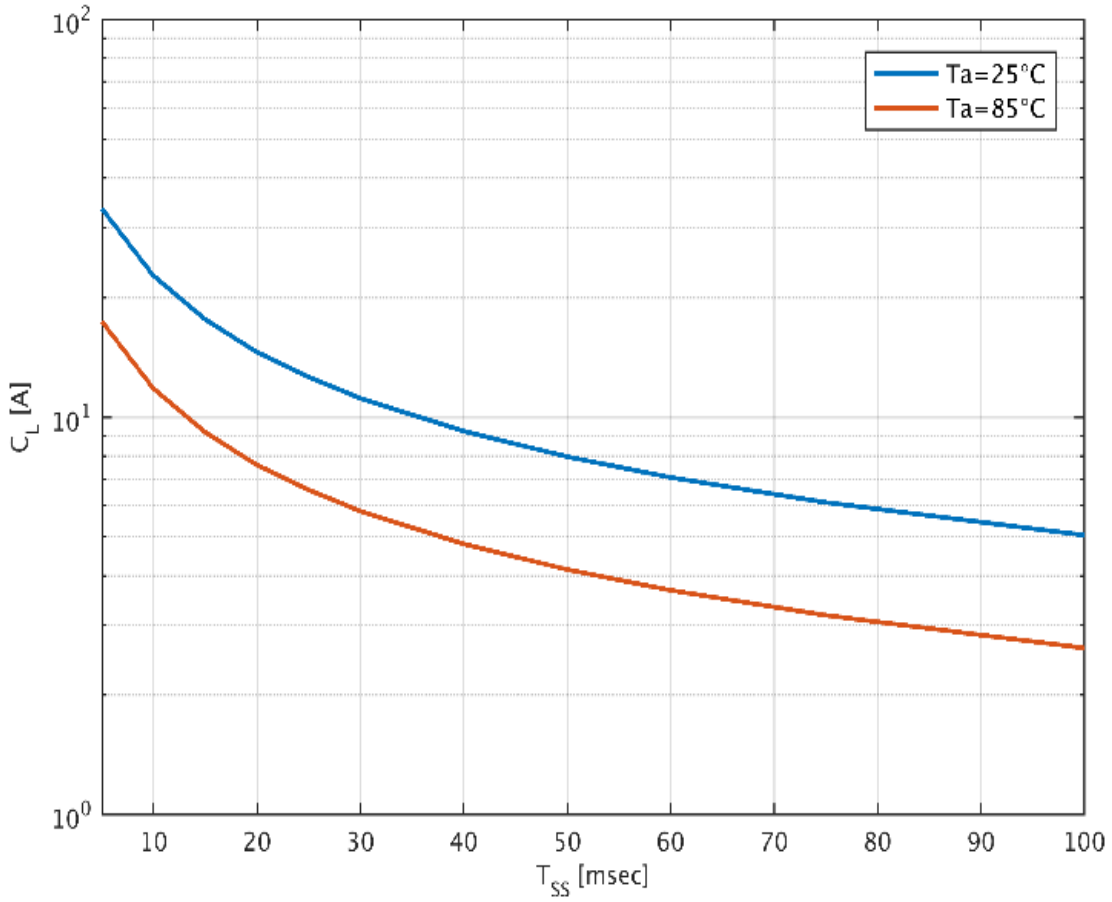
$$T_{jmax}(t) = T_a + \frac{R(t)V_{DS}I_D(T_a)}{1 - R(t)V_{DS}\alpha_T}$$

the condition for thermal instability:

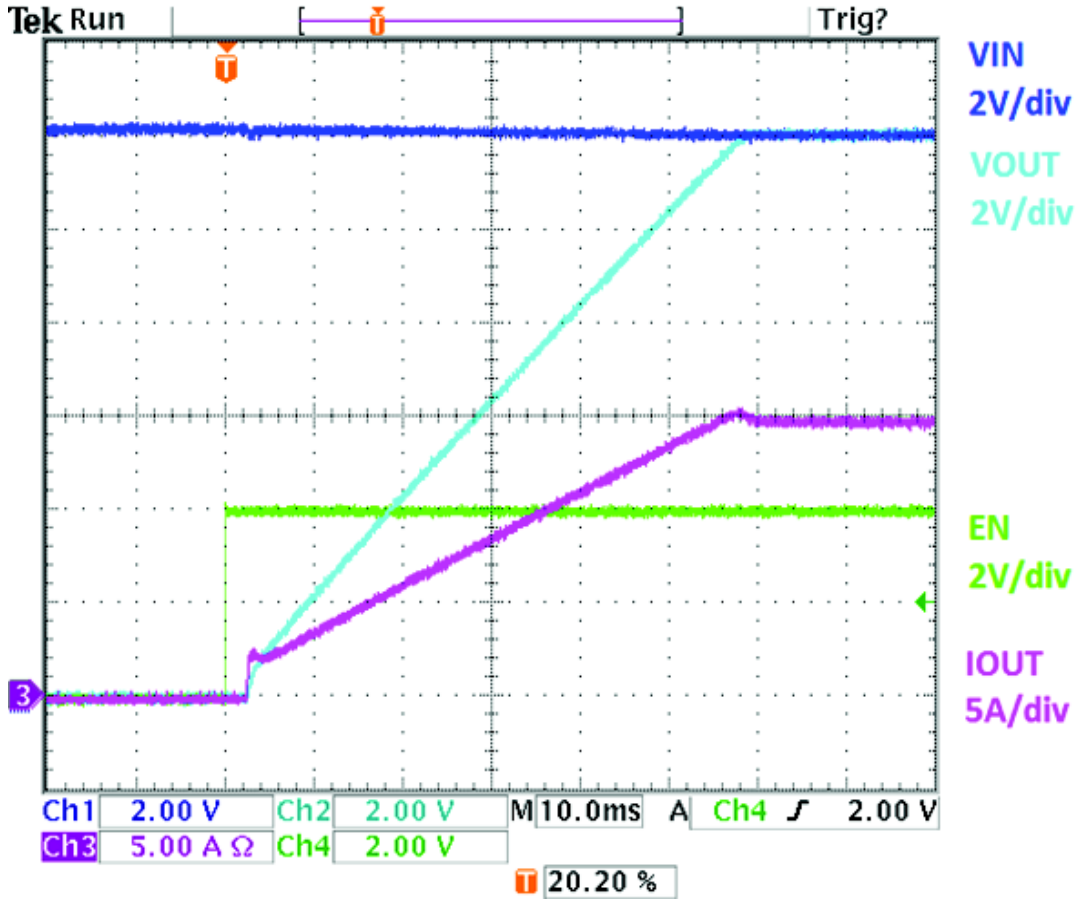
$$\alpha_T \geq \frac{1}{R(t)V_{DS}} = \frac{1}{S}$$



Optimized Real Case



The 1st stage current limit level for different soft-start time(5-100ms）



NCP81295 power on waveforms with load of 0.85mΩ and 4700μF (T_{SS}=50ms）

Conclusion

A 3-stage foldback current limit method was presented for hot-swap and E-Fuse ICs. This method included both of transient thermal characteristic and electro-thermal instability considerations and achieved pseudo constant power control in linear mode operation of build-in MOSFET.

With the emerging of wide SOA MOSFET technology and high power 12/48V bus system in server/telecom, this method will have a wider application in the design of hot-swap and E-Fuse ICs.

Thanks you!